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Washington, D.C. 20231

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

Attorney Docket No.	:	MICRON.009DV1
Applicant(s)	:	Schuegraf, et al.
For	:	SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR
Attorney	:	James B. Bear
"Express Mail" Mailing Label No.	:	EI237892187US
Date of Deposit	:	September 17, 1997

I hereby certify that the accompanying

Transmittal in Duplicate; Specification in eleven (11) pages; four (4) sheets of drawings; Check for Filing Fee; Return Prepaid Postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and are addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231.

Don King

ASA-3133:smn
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** U.S. PATENT AGENT

DIVISIONAL PROGRAM APPLICATION TRANSMITTAL FORM

ANTICIPATED CLASSIFICATION OF THIS APPLICATION
Class: 437 Subclass: 067.000
PRIOR APPLICATION
Examiner: T. Dang Art Unit: 1104

To the Assistant Commissioner for Patents:

This is a Request for filing a divisional application under 37 CFR 1.60, of pending prior Application No. 08/547,620, filed on October 24, 1995, of Klaus Schuegraf and Aftab Ahmad for SHALLOW TRENCH ISOLATION AND USING LOW DIELECTRIC CONSTANT INSULATOR.

(X) Enclosed is a copy of the latest inventor-signed prior application, including the drawings and the oath or declaration as originally filed. I hereby verify that the attached papers are a true copy of the latest inventor-signed prior Application No. 08/547,620 as originally filed on October 24, 1995, and further that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

(X) The filing fee is calculated below:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	FEE
Basic Fee			$770	$770
Total Claims	6 - 20 =	0 ×	$22	$0
Independent Claims	1 - 3 =	0 ×	$80	$0
If application contains any multiple dependent claims(s), then add			$260	$0
		TOTAL FILING FEE		$770

(X) The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. 11-1410. A duplicate copy of this sheet is enclosed.

(X) A check in the amount of $770 is enclosed.

(X) Cancel in this application original Claims 1-10 and 17-20 of the prior application before calculating the filing fee.

(X) Amend the specification by inserting the following before the first line: "This application is a divisional of U.S. Patent Application No. 08/547,620, filed October 24, 1995."

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(X) The prior application is assigned of record to MICRON TECHNOLOGIES, INC.

(X) Return prepaid postcard.

Address all future communications to:

James B. Bear
Knobbe, Martens, Olson & Bear, LLP
620 Newport Center Drive
Sixteenth Floor
Newport Beach, CA 92660

Date: September 17, 1997

Signature: ______________________
James B. Bear
Registration No. 25,221
Attorney of Record

ASA-3119 smn
091197

MICRON.004A
GVH/JBB/ASA
2816

UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APRIL 07, 1996

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UNITED STATES PATENT AND TRADEMARK OFFICE
NOTICE OF RECORDATION OF ASSIGNMENT DOCUMENT

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RECORDATION DATE: 10/24/1995

REEL/FRAME: 7746/0914
NUMBER OF PAGES: 3

BRIEF: ASSIGNMENT OF ASSIGNOR'S INTEREST (SEE DOCUMENT FOR DETAILS).

ASSIGNOR:
SCHUEGRAF, KLAUS F.

DOC DATE: 10/19/1995

ASSIGNOR:
AHMAD, AFTAB

DOC DATE: 10/19/1995

ASSIGNEE:
MICRON TECHNOLOGY, INC.
8000 FEDERAL WAY
BOISE, IDAHO 83707

SERIAL NUMBER: 08547620
PATENT NUMBER:

FILING DATE: 10/24/1995
ISSUE DATE:

DOCKETED ON: APR 19 1996
BY: TN VERIFIED BY:
ACTION: none
DUE DATE:
FINAL DEADLINE:
ATTY: GVH/JBB/ASA
ATTORNEY VERIFICATION OF DUE DATE AND FINAL DEADLINE:

LAWAN FLETCHER, EXAMINER
ASSIGNMENT DIVISION
OFFICE OF PUBLIC RECORDS

Client Code: MICRON.009A

12-18-1995

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40-583 A

SHEET 08/547620

TO THE ASSISTANT COMMISSION ed original documents or copy thereof.

1. Name of conveying party(ies): (If multiple assignors, list numerically)
   1. Klaus F. Schuegraf
   2. Aftab Ahmad

   Additional name(s) of conveying party(ies) attached?
   ( ) Yes (X) No

2. ... and address of receiving party(ies):

   Name: Micron Technology, Inc.
   Internal Address:
   Street Address: 8000 Federal Way
   City: Boise **State:** ID **ZIP:** 83707

   Additional name(s) of receiving party(ies) attached?
   ( ) Yes (X) No

3. Nature of conveyance:

   (x) Assignment
   ( ) Merger
   ( ) Security Agreement
   ( ) Change of Name
   ( ) Other:

   Execution Date: (If multiple assignors, list execution dates in numerical order corresponding to numbers indicated in 1 above)
   October 19, 1995

4. Application number(s) or Patent number(s):

   (x) Application(s) filed herewith Execution Date(s):
   October 19, 1995

   ( ) Patent Application No.: /
   Filing Date:

   ( ) Patent No.:
   Issue Date:

   Additional numbers attached? ( ) Yes (X) No

5. Name and address of party to whom correspondence concerning document should be mailed:

   Name: James B. Bear
   KNOBBE, MARTENS, OLSON & BEAR
   Internal Address: Sixteenth Floor
   Street Address: 620 Newport Center Drive
   City: Newport Beach **State:** CA **ZIP:** 92660
   Attorney's Docket No.: MICRON.009A

6. Total number of applications and patents involved: one

7. Total fee (37 CFR 3.41): $40

   (X) Enclosed
   (X) Authorized to be charged to deposit account if any additional fees are required, or to credit any overpayment

8. Deposit account number: 11-1410

   Please charge this account for any additional fees which may be required, or credit any overpayment to this account.

   (Attach triplicate copy of this page if paying by deposit account.)

9. Statement and signature.

   To the best of my knowledge and belief, the foregoing information is true and correct, and any attached copy is a true copy of the original document.

   James B. Bear
   Name of Person Signing

   Signature

   10/24/95
   Date

   25,221
   Registration No.

66080 U.S. PTO
12/13/95

Total number of pages including cover sheet, attachments and document: 3

Mail documents to be recorded with required cover sheet information to:

Assistant Commissioner for Patents
Box Assignments
Washington, D.C. 20231

DLA-1347:vm
102495

270 MM 12/05/95 08547620 1 581 40.00 OP

Application No.: Unknown
Filing Date: Herewith

ASSIGNMENT

WHEREAS, We, Klaus F. Schuegraf, a United States citizen, residing at 2000 White Pine Lane, Boise, ID 83706, Aftab Ahmad, a United States citizen, residing at 3426 S. Pimmet Place, Boise, ID 83706 have invented certain new and useful improvements in a SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR for which we have executed an application for Letters Patent in the United States, on even date herewith;

AND WHEREAS, Micron Technology, Inc. (hereinafter "ASSIGNEE"), a Delaware Corporation, with its principal place of business at 8000 S. Federal Way, Boise, ID 83707, desires to acquire the entire right, title, and interest in and to the said improvements and the said Application:

NOW, THEREFORE, in consideration of the sum of One Dollar ($1.00) each to us in hand paid, and other good and valuable consideration, the receipt of which is hereby acknowledged, we, the said inventors, do hereby acknowledge that we have sold, assigned, transferred and set over, and by these presents do hereby sell, assign, transfer and set over, unto the said ASSIGNEE, its successors, legal representatives and assigns, the entire right, title, and interest throughout the world in, to and under the said improvements, and the said application and all divisions, renewals and continuations thereof, and all Letters Patent of the United States which may be granted thereon and all reissues and extensions thereof, and all rights of priority under International Conventions and applications for Letters Patent which may hereafter be filed for said improvements in any country or countries foreign to the United States, and all Letters Patent which may be granted for said improvements in any country or countries foreign to the United States and all extensions, renewals and reissues thereof; and we hereby authorize and request the Commissioner of Patents of the United States, and any Official of any country or countries foreign to the United States, whose duty it is to issue patents on applications as aforesaid, to issue all Letters Patent for said improvements to the said ASSIGNEE, its successors, legal representatives and assigns, in accordance with the terms of this instrument.

AND WE HEREBY covenant and agree that we will communicate to the said ASSIGNEE, its successors, legal representatives and assigns, any facts known to us respecting said improvements, and testify in any legal proceeding, sign all lawful papers, execute all divisional, continuing and reissue applications, make all rightful oaths and generally do everything possible to aid the said ASSIGNEE, its successors, legal representatives and assigns, to obtain and enforce proper patent protection for said improvements in all countries.

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 19th day of Oct, 1995

Klaus F Schuegraf
Klaus F. Schuegraf

STATE OF
ss.
COUNTY OF

On Oct 19, 1995, before me, Deanne Schildan personally appeared Klaus F. Schuegraf personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL] DEANNE SCHILDAN NOTARY PUBLIC STATE OF IDAHO

Deanne Schildan
Signature

IN TESTIMONY WHEREOF, I hereunto set my hand and seal this 19 day of Oct., 1995

[signature]

Aftab Ahmad

STATE OF

] ss.

COUNTY OF

On Oct. 19/95, before me, Deanne Schildan personally appeared Aftab Ahmad personally known to me (or proved to me on the basis of satisfactory evidence) to be the person(s) whose name(s) is/are subscribed to the within instrument, and acknowledged to me that he executed the same in his authorized capacity(ies), and that by his signature(s) on the instrument the person(s), or the entity upon behalf of which the person(s) acted, executed the instrument.

WITNESS my hand and official seal.

[SEAL]

DEANNE SCHILDAN NOTARY PUBLIC STATE OF IDAHO

Deanne Schildan

Signature

DLA-1[illegible]4:vm
10059[illegible]

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant	:	Klaus F. Schuegraf et al.
App. No.	:	Unknown
Filed	:	Herewith
For	:	SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR
Examiner	:	Unknown

ESTABLISHMENT OF RIGHT OF ASSIGNEE TO TAKE ACTION
AND
REVOCATION AND POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

The undersigned is empowered to act on behalf of the assignee below (the "Assignee"). A true copy of the original Assignment of the above-captioned application from the inventor(s) to the Assignee is attached hereto. This Assignment represents the entire chain of title of this invention from the Inventor(s) to the Assignee. I have reviewed this Assignment, and to the best of the Assignee's knowledge and belief, the Assignee is the owner of the entire right, title and interest in the above-referenced application.

I declare that all statements made herein are true, and that all statements made upon information and belief are believed to be true, and further, that these statements were made with the knowledge that willful, false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001, and that willful, false statements may jeopardize the validity of the application, or any patent issuing thereon.

The undersigned hereby revokes any previous powers of attorney in the subject application, and hereby appoints Louis J. Knobbe, Registration No. 18,780; Don W. Martens, Registration No. 21,107; Gordon H. Olson, Registration No. 20,319; James B. Bear, Registration No. 25,221; Darrell L. Olson, Registration No. 28,247; William B. Bunker, Registration No. 29,365; William H. Nieman, Registration No. 30,201; Lowell Anderson, Registration No. 30,990; Arthur S. Rose, Registration No. 28,038; James F. Lesniak, Registration No. 25,240; Ned A. Israelsen, Registration No. 29,655; Drew S. Hamilton, Registration No. 29,801; Jerry T. Sewell, Registration No. 31,567; John B. Sganga, Jr., Registration No. 31,302; Edward A. Schlatter, Registration No. 32,297; Gerard von Hoffmann, Registration No. 33,043; Joseph R. Re, Registration No. 31,291; John M. Carson,

App. No. : Unknown
Filed : Herewith

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Please direct all communications relative to said application to the following correspondence address:

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MICRON TECHNOLOGY, INC.

Dated: Oct. 16, 1995

By: Bryan Farney
W. Bryan Farney

Title: Vice President Legal Affairs & General Counsel

Address: 8000 S. Federal Way
Boise, ID 83707

DLA-1335:vm
100595

SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR

Field of the Invention

The invention relates generally to silicon integrated circuit design and process technology. In particular, the invention pertains to trench isolation process technology.

Background of the Invention

Implementing electronic circuits involves connecting isolated devices through specific electronic paths. In silicon integrated circuit fabrication it is necessary to isolate devices from one another which are built into the same silicon matrix. They are subsequently interconnected to create the desired circuit configuration. In the continuing trend toward higher device densities, parasitic interdevice currents become more problematic, thus isolation technology has become one of the most critical aspects of contemporary integrated circuit fabrication.

Over the last few decades a variety of successful isolation technologies have been developed to address the requirements of different integrated circuit types such as NMOS, CMOS and bipolar. In general, the various isolation technologies exhibit different attributes with respect to such characteristics as minimum isolation spacing, surface planarity, process complexity and defect density generated during isolation processing. Moreover, it is common to trade off some of these characteristics when developing an isolation process for a particular integrated circuit application.

In metal-oxide-semiconductor (MOS) technology it is necessary to provide an isolation structure that prevents parasitic channel formation between adjacent devices, such devices being primarily NMOS or PMOS transistors or CMOS circuits. The most widely used isolation technology for MOS circuits has been that of LOCOS isolation, an acronym for LOCal Oxidation of Silicon. LOCOS isolation essentially involves the growth of a recessed or semirecessed oxide in unmasked non-active or field regions of the silicon substrate. This so-called field oxide is generally grown thick enough to lower any parasitic capacitance occurring over these regions, but not so thick as to cause step coverage problems. The great success of LOCOS isolation

technology is to a large extent attributed to its inherent simplicity in MOS process integration, cost effectiveness and adaptability.

In spite of its success, several limitations of LOCOS technology have driven the development of alternative isolation structures. A well-known limitation in LOCOS isolation is that of oxide undergrowth at the edge of the mask which defines the active regions of the substrate. This so-called bird's beak (as it appears) poses a limitation to device density, since that portion of the oxide adversely influences device performance while not significantly contributing to device isolation. Another problem associated with the LOCOS process is the resulting circuit planarity or lack thereof. For submicron devices, planarity becomes an important issue, often posing problems with subsequent layer conformality and photolithography.

Trench isolation technology has been developed in part to overcome the aforementioned limitations of LOCOS isolation for submicron devices. Refilled trench structures essentially comprise a recess formed in the silicon substrate which is refilled with a dielectric material. Such structures are fabricated by first forming submicron-sized trenches in the silicon substrate, usually by a dry anisotropic etching process. The resulting trenches typically display a steep sidewall profile as compared to LOCOS oxidation. The trenches are subsequently refilled with a dielectric such as chemical vapor deposited (CVD) silicon dioxide (SiO_2). They are then planarized by an etchback process so that the dielectric remains only in the trench, its top surface level with that of the silicon substrate. The etchback process is often performed by etching photoresist and the deposited silicon dioxide at the same rate. The top surface of the resist layer is highly planarized prior to etchback through application of two layers of resist, and flowing the first of these layers. Active regions wherein devices are fabricated are those that were protected from etch when the trenches were created. The resulting structure functions as a device isolator having excellent planarity and potentially high aspect ratio beneficial for device isolation. Refilled trench isolation can take a variety of forms depending upon the specific application; they are generally categorized in terms of the trench dimensions: shallow trenches (< 1 μm), moderate depth trenches (1-3 μm), and deep, narrow trenches (> 3 μm deep, < 2 μm wide). Shallow Trench Isolation (STI) is used primarily for isolating devices of the same type

and is often considered an alternative to LOCOS isolation. Shallow trench isolation has the advantages of eliminating the birds beak of LOCOS and providing a high degree of surface planarity.

The basic trench isolation process is, however, subject to drawbacks, one of these being void formation in the trench during dielectric refill. Such voids are formed when the refilling dielectric material forms a constriction near the top of a trench, preventing flow of the material into the trench interior. Such voids compromise device isolation as well as the overall structural integrity. Unfortunately, preventing void formation during trench refill often places minimum size constraints on the trenches themselves, which may compromise device packing density or device isolation. For example, a key parameter measuring device isolation is the field threshold voltage between adjacent devices, that is, the voltage necessary to create a parasitic channel beneath a field oxide region linking adjacent devices. The field threshold voltage is influenced by a number of physical and material properties of the trench isolator such as insulator thickness, dielectric constant ε, substrate doping, field implant dose and substrate bias. Thus, a principal difficulty in decreasing the trench depth is the compromise in device isolation. Clearly, it is highly desirably to develop a shallow trench isolation process which overcomes the problem of void formation while providing effective device isolation.

Summary of the Invention

It is an object of the present invention to provide a trench isolation process which alleviates the problem of void formation during dielectric refill. It is another object of the present invention to provide a trench isolator having reduced dimensions, advantageous for device density and wafer planarity. It is a further object of the present invention to provide a shallow trench isolator having enhanced device isolation characteristics.

In accordance with one aspect of the present invention, a process for isolating devices on a semiconductor substrate comprises first removing portions of the semiconductor substrate, thereby forming recesses preferably having a trench profile. The trenches are then refilled with a material having a dielectric constant lower than the dielectric constant of silicon dioxide which is about 3.9. Using a low-ε dielectric

material allows the trench dimensions to be reduced while still providing effective device isolation characteristics. Preferably, the dielectric material comprises a halide-doped glass such as Fluorine-doped SiO_2. To insure against device contamination, the invention further comprises forming a barrier layer over the trenches prior to refilling them with the low-ε dielectric material.

In accordance with another aspect of the present invention, an isolation structure in a semiconductor substrate comprises a recessed trench formed in the semiconductor substrate and a material having a low dielectric constant filling the trench. The trench structure preferably has a depth less than 250 nm, and furthermore comprises a barrier layer disposed between the interior trench surface and the dielectric material. The dielectric material preferably has a dielectric constant lower than about 3.9, and may comprise a Fluoride-doped silicon dioxide composition.

In accordance with yet another aspect of the present invention, a method of reducing the formation of voids in a refilled trench isolation process comprises forming trenches having an aspect ratio less than about 2:1, and then refilling the trenches with a material having a dielectric constant less than the dielectric constant of silicon dioxide. The trenches preferably have a depth of less than 200 nm, and are refilled with a material comprising a Fluorine-doped silicon dioxide composition.

These and other aspect and attributes of the present invention will become more fully apparent with the following detailed description and accompanying figures.

Brief Description of the Drawings

Figures 1A-1C are schematic sections illustrating an exemplary shallow trench isolation process.

Figure 2 is a schematic section of a trench refill having a void.

Figure 3 is a schematic section illustrating an embodiment of the present shallow trench isolation process.

Detailed Description of the Invention

In accordance with the principles of the present invention, an improved shallow trench isolation technology utilizes a trench that is shallower than prior art trenches, and yet provides the same degree of device isolation. The shallower trench helps prevent the formation of voids during dielectric refill. However, despite the smaller

dimensions of the present inventive trench, equivalent device isolation is achieved through use of a dielectric refill having a lower dielectric constant ε than in prior art isolation trenches. To better illustrate these inventive principles, a brief description of an exemplary STI process is provided first hereinbelow.

An exemplary STI process may comprise first a masking, patterning and dry etch process, producing trenches in the silicon substrate as shown in Figure 1A. The semiconductor substrate 10 is masked and patterned to expose the regions of the substrate to be etched. The mask 12 may for example comprise a resist layer which is resistant to the dry anisotropic etch used to create the trenches. The mask 12 may be patterned by conventional photolithographic means to define the regions of the substrate 10 to have trenches formed therein. The trenches 14 are formed by an anisotropic dry etch, such as a plasma or reactive ion etch. A preferred characteristic of the trenches 14 is the steep sidewall profile as compared to conventional LOCOS processes.

After the trenches 14 are formed, the mask 12 is removed by selective etching or chemical mechanical polishing and the trenches are refilled with a dielectric material 16, as shown in Figure 1B. A preferred dielectric refill material for STI is chemical vapor deposited silicon dioxide (CVD-SiO_2) due to its high quality and excellent conformality. Conformality is particularly important because the refilled material must be supplied to fill trenches having relatively high aspect ratios (height:width>1).

Following the trench refill 16, the top surface of the substrate 10 is planarized by an etchback process, typically also performed using a chemical/mechanical polish. Prior to etchback, the substrate 10 may be coated with a layer of photoresist (not shown) in order to provide a planar surface with which to begin the etchback. The etchback itself provides a planarized substrate surface 18, having dielectric material 16 filling the trenches 14 up to and level with the top surface 18.

As shown in Figure 2, a common problem associated with trench refill isolation is the formation of voids in the trenches. During refill of the trench 14 with dielectric material 16, the trench 14 often becomes constricted near the top of the trench, thereby preventing complete refill of the trench, resulting in a void 20. The void 20 lowers

the isolation characteristics of the refilled trench in addition to introducing structural instabilities in subsequent processes. Increasing the trench width can alleviate void formation, however it also undesirably decreases device density.

In accordance with the principles of the present invention, void formation is alleviated by decreasing trench depth. Utilizing shallower trenches decreases the possibility of void formation and favorably increases surface planarity of the final refilled trench structure. For example in a typical DRAM application, a trench in accordance with the present invention may have dimension of approximately 200 nm deep and 250 nm wide while prior art trenches typically have dimensions of approximately 275 nm deep and 350 nm wide. However, as is well known in the art, a key parameter measuring device isolation is the field threshold voltage between adjacent devices, that is, the voltage necessary to create a parasitic channel beneath a field oxide region linking adjacent devices. The field threshold voltage is influenced by a number of physical and material properties of the trench isolator such as insulator thickness, dielectric constant ε, substrate doping, field implant dose and substrate bias. Thus, a principal difficulty in decreasing the trench depth is the compromise in device isolation.

To circumvent this problem, the shallow trench isolation of the present invention maintains effective device isolation in a shallower trench by utilizing dielectric materials having a lower dielectric constant than used in the prior art. For a given trench geometry, the field threshold voltage is a decreasing function of the field dielectric constant. Thus, to compensate for smaller trench dimensions, the present invention utilizes dielectric materials having lower dielectric constant. A possible dielectric material is a low index glass such as a halide-doped silicon dioxide, deposited by introducing the halide during CVD of silicon dioxide. For example, $F:SiO_2$ possesses a dielectric constant of approximately 3.2, while typical CVD-SiO_2 has a dielectric constant of about 3.9. Use of such materials allows a relative decrease in trench depth by about 20 %.

Fluorine or other elements comprising a reduced dielectric constant material may however cause deleterious effects on neighboring devices if they diffuse into adjacent active areas. Therefore, a preferred embodiment of the present invention also

incorporates a diffusion barrier layer lining the trench so as to prevent dopant migration into the silicon substrate. Use of a preferred barrier layer in the form of a grown oxide or nitride film, or a deposited stoichiometric or non-stoichiometric oxide or nitride film inhibits contamination of the isolation field-effect transistor, thereby preserving desirable characteristics such as a high threshold voltage. The integrated devices subject to isolation are also protected by the barrier layer from contamination.

In accordance with the aforementioned principles, a preferred shallow trench isolation may for example comprise the following process steps illustrated in Figures 3A-3D. As shown in Figure 3A, the silicon wafer 10 is first covered by a mask 12, such as a resist or silicon oxide/nitride bilayer, and then patterned and etched to define the field isolation regions. The wafer is then subject to a dry anisotropic etch such as a halide plasma complex, thereby forming the trenches 22 in the silicon substrate 10. As mentioned earlier, in comparison to the prior art trench isolation, the trenches of the present invention are about 200 nm deep, shallower than the prior art by about 20 %.

As mentioned previously, to avoid contamination of substrate regions adjacent to the trenches 22, it is preferable to form a barrier layer 24 over the trenches 22 prior to dielectric refill as shown schematically in Figure 3B. The barrier layer 24 may for example comprise a silicon oxide or nitride film grown in an appropriate ambient or a chemical vapor deposited oxide or nitride film at least 5 nm thick. The barrier layer 24 functions to prevent diffusion of dopants deposited during the subsequent dielectric refill process. Although in general nitride forms a superior diffusion barrier to oxide, the higher dielectric constant of nitride should be considered in the overall isolation structure. It may be for example, that oxide performs adequately as a diffusion barrier while having the advantage of a lower dielectric constant than nitride. Thus, barrier layer thickness and dielectric constant should be considered in the overall trench design.

A shown in Figure 3C, the trenches 22 are refilled with a dielectric material 26 having a low dielectric constant ε of about 3.3. As mentioned previously, the use of a low dielectric constant material lowers the gate capacitance of the isolation field-

effect transistor, thereby raising the threshold voltage. A CVD-SiO_2 doped with a halide such as Fluorine is a presently preferred material.

To complete the trench structure, a planarizing step is performed as shown in Figure 3D. A planarizing process may for example comprise depositing and reflowing a resist layer to attain a planar top surface, followed by an etchback procedure to remove material down to the substrate surface. While the planarizing process may proceed in accordance with well-known processes, the present preferred isolation is advantageous because the shallower trench structures and consequent thinner refilled layers allow for a greater degree of planarity.

Thus, the present invention provides several advantages over the prior art by avoiding cavities in the trenches, providing more effective device isolation using low-ε materials and having a greater degree of planarity in the final trench structure.

Although described above with reference to the preferred embodiments, modifications within the scope of the invention may be apparent to those skilled in the art, all such modifications are intended to be within the scope of the appended claims.

WHAT IS CLAIMED IS:

1. A process for isolating devices on a semiconductor substrate comprising the steps of:

removing predetermined portions of the semiconductor substrate forming recesses therein; and

refilling the portions of the semiconductor substrate with a material having a dielectric constant lower than the dielectric constant of silicon dioxide.

2. The process of Claim 1, wherein the step of removing portions of the semiconductor wafer comprises forming trenches in the semiconductor wafer.

3. The process of Claim 2, wherein the trenches have a depth of less than 200 nm.

4. The process of Claim 3, wherein the trenches have an aspect ratio of less than 2:1.

5. The process of Claim 1, wherein the material having a dielectric constant lower than that of silicon dioxide comprises a halide-doped silicon dioxide composition.

6. The process of Claim 5, wherein the halide-doped silicon dioxide complex comprises a Fluorine-doped silicon dioxide complex.

7. The process of Claim 1, wherein the refilling material has a dielectric constant less than about 3.9.

8. The process of Claim 1, further comprising forming a barrier layer over the semiconductor substrate prior to the step of refilling portions of the semiconductor substrate.

9. The process of Claim 8, wherein the barrier layer comprises a silicon dioxide composition.

10. The process of Claim 8, wherein the barrier layer comprises a silicon nitride composition.

11. An isolation structure in a semiconductor substrate comprising:

a recessed portion formed therein in the semiconductor substrate; and

a dielectric material filling the recessed portion, said dielectric material having a dielectric constant lower than the dielectric constant of silicon dioxide.

12. The isolation structure of Claim 11, wherein the recessed portion comprises a trench structure having an aspect ration of less than 2:1.

13. The isolation structure of Claim 11, wherein the recessed portion comprises a trench structure having a depth of less than 200 nm.

14. The isolation structure of Claim 11, further comprising a barrier layer disposed between the recessed portion of the semiconductor substrate and the dielectric material.

15. The isolation structure of Claim 11, wherein the dielectric material has a dielectric constant lower than 3.9.

16. The isolation structure of Claim 11, wherein the dielectric material comprises a Fluoride-doped silicon dioxide composition.

17. A method of reducing the formation of voids in a refilled trench isolation process comprising the steps of:

forming trenches having an aspect ratio less than 2:1; and

refilling the trenches with a material having a dielectric constant less than the dielectric constant of silicon dioxide.

18. The method of Claim 17, wherein the trenches have a depth of less than 200 nm.

19. The method of Claim 17, wherein the refilling material comprises a Fluorine-doped silicon dioxide composition.

20. The method of Claim 17, wherein the refilling material has a dielectric constant of less than about 3.9.

SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR

Abstract of the Invention

A shallow trench isolation is disclosed wherein the trench depth is reduced beyond that achieved in prior art processes. The reduced trench depth helps to eliminate the formation of voids during the trench refill process and provides for greater planarity in the final isolation structure. Effective device isolation is achieved with a reduced trench depth by utilizing refilling dielectric materials having low dielectric constant.

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Fig. 1A
(PRIOR ART)

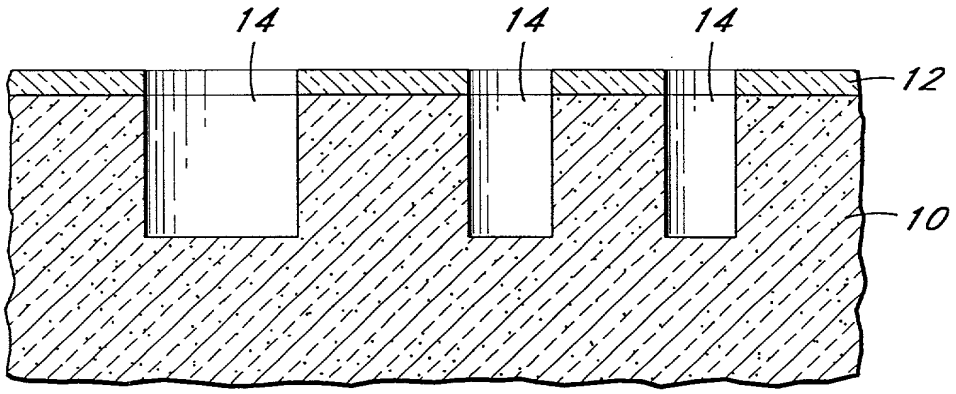


Fig. 1B
(PRIOR ART)

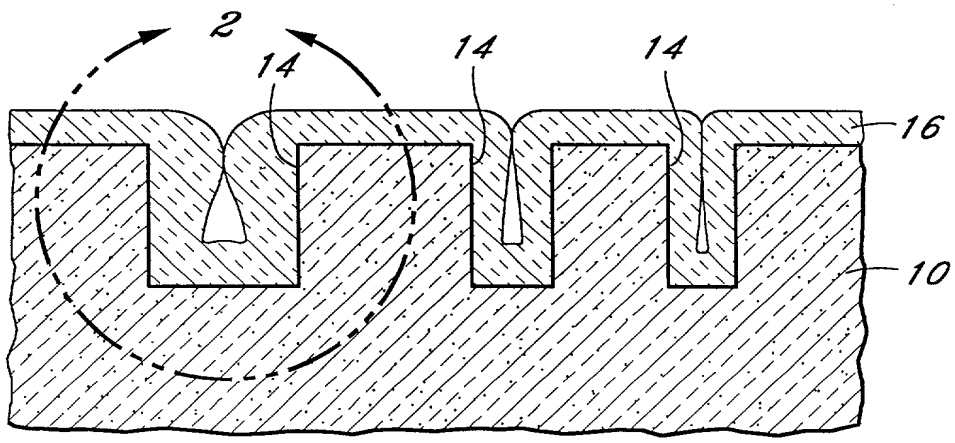


Fig. 1C
(PRIOR ART)

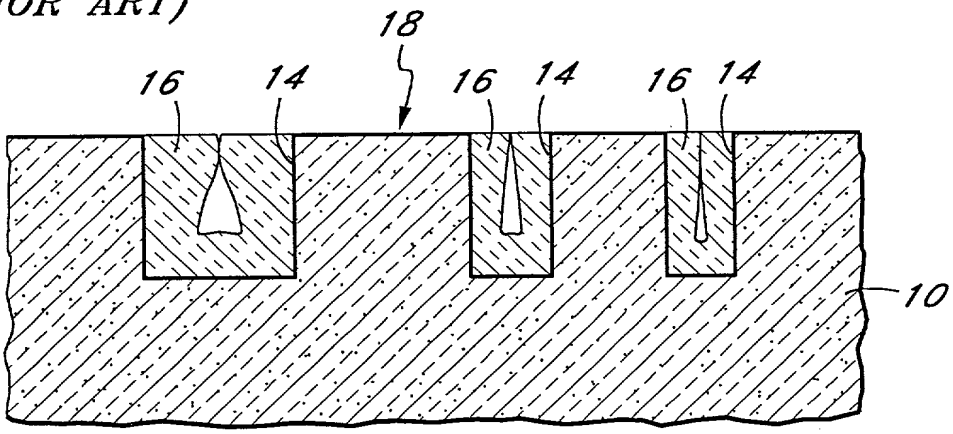


Fig. 2
(PRIOR ART)

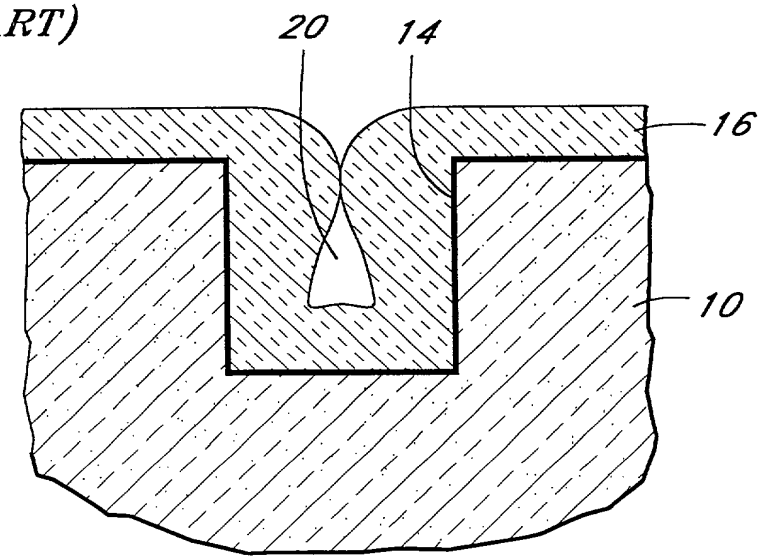


Fig. 3A

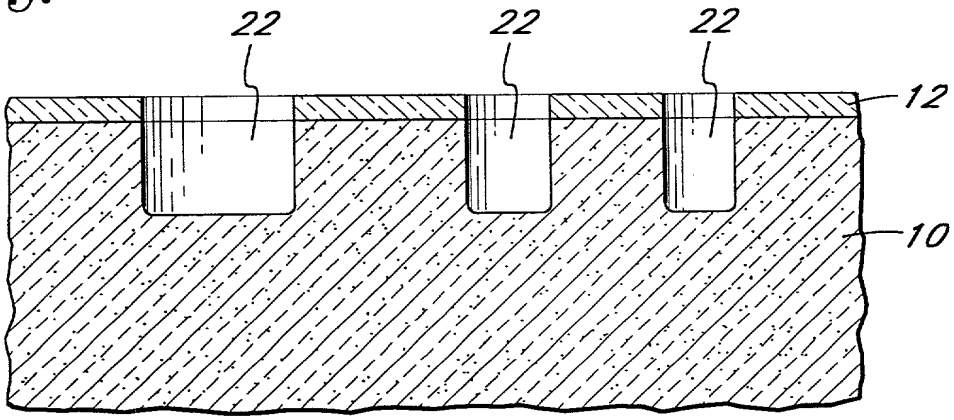


Fig. 3B

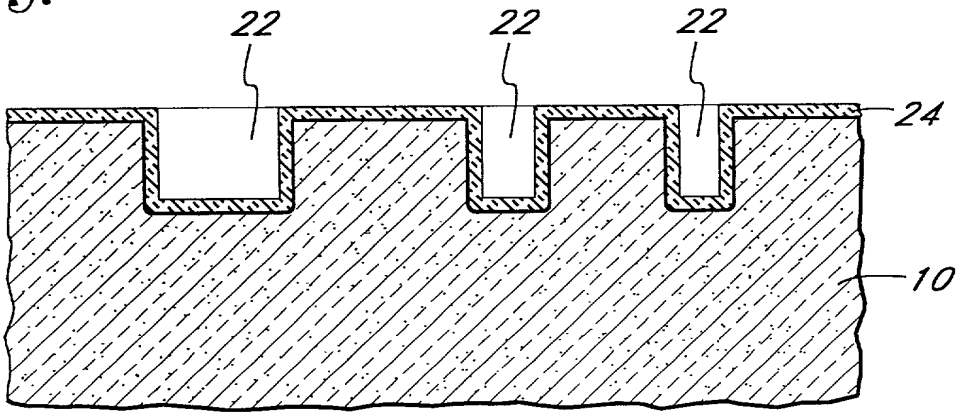


Fig. 3C

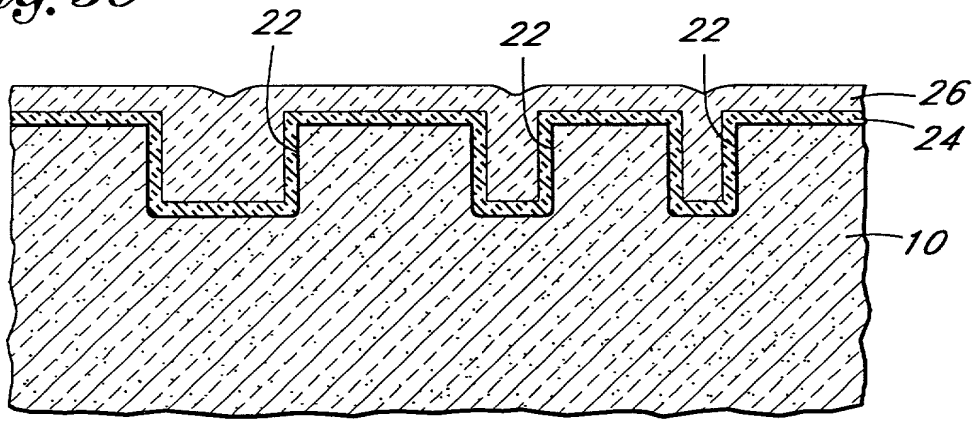
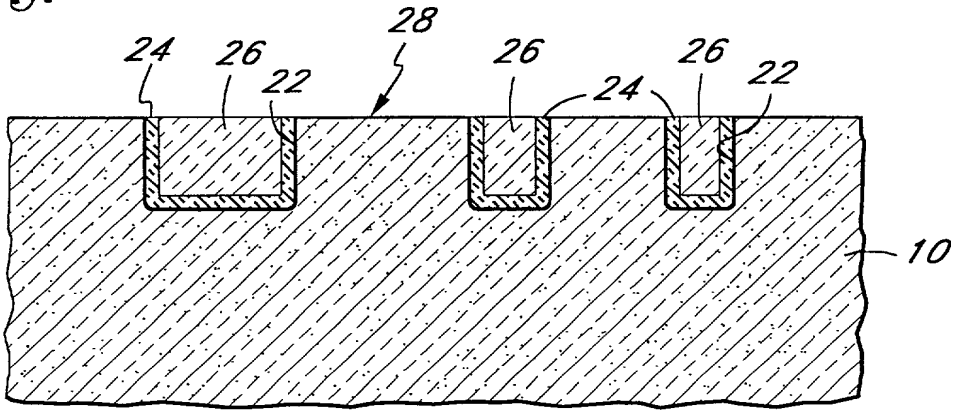


Fig. 3D



DECLARATION - USA PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am an original, first and joint inventor of the subject matter which is claimed and for which a patent is sought on the invention entitled SHALLOW TRENCH ISOLATION USING LOW DIELECTRIC CONSTANT INSULATOR; the specification of which is attached hereto;

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above;

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56;

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful, false statements may jeopardize the validity of the application or any patent issued thereon.

- -

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